CLAIMS

1. Apparatus for testing an integrated circuit to determine if 1/f noise of a circuit to be tested on said integrated circuit is within specifications, comprising:

a. a mechanism for applying an offset inside a chopper stabilized circuit forming part of said circuit to be tested, and

b. a circuit for checking whether the output of said chopper stabilized circuit is within specification for a chopper stabilized circuit that is working properly, whereby one may infer that 1/f noise is within specifications.

Sub A1

2. Apparatus of claim 1 in which said offset has a value greater than expected in normal use with the chopper stabilized circuit.

3. Apparatus of claim 1 in which the circuit to be tested passes a 1/f noise test if the output of the chopper stabilized circuit is within specifications for a properly working chopper stabilized circuit.

4. Apparatus of claim 1 in which said chopper stabilized circuit is a chopper stabilized amplifier.

5. A method for testing an integrated circuit to determine if 1/f noise of a circuit to be tested on said integrated circuit is within specifications, comprising:

a. applying an offset inside a chopper stabilized circuit forming part of said circuit to be tested, and

b. checking whether the output of said chopper stabilized circuit is within specification for a chopper stabilized circuit that is working properly, whereby one may infer that 1/f noise is within specifications.

Sub A2

6. The method of claim 5 in which said offset has a value greater than expected in normal use with the chopper stabilized circuit.

7. The method of claim 6 in which the circuit to be tested passes a 1/f noise test if the output of the chopper stabilized circuit is within specifications for a properly

working chopper stabilized circuit.

8. The method of claim 5 in which said chopper stabilized circuit is a chopper stabilized amplifier.

9. A method of testing for 1/f noise performance in less than 1/f time comprising the step of using proper offset removal of a chopper stabilized circuit as a surrogate for measuring for 1/f noise.

10. A method of designing an integrated circuit, comprising the step of providing access at the output and control of internal offset of a chopper stabilized circuit.

11. A method of fabricating an integrated circuit, comprising the step of providing access at the output and control of internal offset of a chopper stabilized circuit.

12. A method of testing an integrated circuit, comprising the steps of controlling offset at a chopper stabilized circuit and using offset removal as a surrogate for 1/f noise performance.